Exhibit E

REDACTED
IN ITS ENTIRETY

Exhibit F

REDACTED
IN ITS ENTIRETY

Exhibit G

Jennifer Pierce

From: VanderZanden, Brian [bvanderzanden@orrick.com]
Sent: Monday, September 17, 2007 9:29 PM
To: Jonathan Lamberson
Cc: Michael Headley
Subject: RE: PI/FC - Horowitz demonstratives

Jonathan,

That's correct. We will not rely upon any TEA2262 demonstratives.

-----Original Message-----
From: Jonathan Lamberson [mailto:Lamberson@fr.com]
Sent: Monday, September 17, 2007 6:21 PM
To: VanderZanden, Brian
Cc: Michael Headley
Subject: RE: PI/FC - Horowitz demonstratives

Brian,

Can you confirm that the following are also typos:

DD842, DD860, DD878, DD879, DD880

All of these demonstratives mention the TEA2262, which we understand Fairchild is no longer asserting. These slides fall in the ranges you identified in your letter of tonight.

Thank you,
Jonathan Lamberson
Fish & Richardson P.C.
500 Arguello St., Ste 500
Redwood City, CA 94063
650-839-5076
lamberson@fr.com

-----Original Message-----
From: VanderZanden, Brian [mailto:bvanderzanden@orrick.com]
Sent: Monday, September 17, 2007 9:13 PM
To: Jonathan Lamberson
Cc: Michael Headley
Subject: RE: PI/FC - Horowitz demonstratives

Jonathan,

DD881-DD832 is a typo. Please disregard.

Additionally, I have confirmed that DD840a is a typo; it should be DD840.

-Brian

-----Original Message-----
From: Jonathan Lamberson [mailto:Lamberson@fr.com]
Sent: Monday, September 17, 2007 5:40 PM
To: VanderZanden, Brian
Cc: Michael Headley
Subject: PI/FC - Horowitz demonstratives

Brian,

You identified the following range in the list of Horowitz demonstratives: DD881-DD832. Can you please clarify what range you intended to identify?

Thank you,
Jonathan Lamberson
Fish & Richardson P.C.
500 Arguello St., Ste 500
Redwood City, CA 94063
650-839-5076
lamberson@fr.com

Exhibit H

REDACTED
IN ITS ENTIRETY

Exhibit I

REDACTED
IN ITS ENTIRETY

Exhibit J

REDACTED
IN ITS ENTIRETY

Exhibit K

REDACTED
IN ITS ENTIRETY

Exhibit L

NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

2007-1082

SYSTEM GENERAL CORP.,

Appellant,

v.

INTERNATIONAL TRADE COMMISSION,

Appellee,

and

POWER INTEGRATIONS, INC.,

Intervenor.

J. Michael Jakes, Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P., of Washington, D.C., argued for appellant. On the brief was Elizabeth A. Niemeyer.

Michelle Walters, Attorney, Office of the General Counsel, United States International Trade Commission, of Washington, DC, argued for appellee. With her on the brief were James M. Lyons, General Counsel, and Wayne W. Herrington, Assistant General Counsel.

Howard G. Pollack, Fish & Richardson P.C. , of Redwood City, California, argued for intervenor. With him on the brief were Michael R. Headley, and Frank E. Scherkenbach, of Boston, Massachusetts. Of counsel were Tamara Fraizer, of Redwood City, California, and William E. Sekyi, of Washington, DC.

Appealed from: United States International Trade Commission

NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

2007-1082

SYSTEM GENERAL CORP.,

Appellant,

v.

INTERNATIONAL TRADE COMMISSION,

Appellee,

and

POWER INTEGRATIONS, INC.,

Intervenor.

JUDGMENT

ON APPEAL from the United States International Trade Commission

In CASE NO(S). 337-TA-541

This CAUSE having been heard and considered, it is

ORDERED and ADJUDGED: AFFIRMED. See Fed. Cir. R. 36

Per Curiam (NEWMAN, Circuit Judge, CLEVENGER, Senior Circuit Judge, and DYK, Circuit Judge).

ENTERED BY ORDER OF THE COURT

DATED: November 19, 2007

/s/ Jan Horbaly
Jan Horbaly, Clerk

Exhibit M

Fairchild Announces Successful Completion of Tender Offer for System General

February 8, 2007 – *South Portland, Maine* – Fairchild Semiconductor (NYSE: FCS), the leading global supplier of power semiconductors, today announced the successful completion of the previously-announced tender offer by one of its wholly owned subsidiaries to acquire up to 100 percent of the outstanding shares of System General Corporation for NT$93 per share. 65,459,517 shares of System General stock were acquired on February 5, 2007, representing 95.59 percent of System General's outstanding shares. The tender offer expired as scheduled and was not extended. The total amount paid for the tendered shares was approximately $US 185.7 million, based on current exchange rates. The purchase price was funded with cash. The company intends to acquire the remaining System General shares through a share swap and merger, provided that certain conditions are met, including regulatory approvals, which the company expects to obtain.

In the transaction, approximately 250 System General employees will join Fairchild, including the current management team. System General will continue normal operations unde its name prior to the share swap, and will operate as an independent business within Fairchild during that time. After the completion of the transaction, Fairchild and System General's management will work together to combine the power conversion businesses of each company and form a single business unit targeting worldwide AC/DC offline power conversion applications.

To learn more contact:

Fairchild Semiconductor:
Patti Olson
Corporate Communications
(800) 341-0392 X 8728
Fax: (207) 775-8161
Email: patti.olson@fairchildsemi.com

About Fairchild Semiconductor:
Fairchild Semiconductor (NYSE: FCS) is the leading global supplier of high-performance power products critical to today's leading electronic applications in the computing, communications, consumer, industrial and automotive segments. As The Power Franchise®, Fairchild offers the industry's broadest portfolio of components that optimize system power. Fairchild's 9,000 employees design, manufacture and market power, analog and mixed signal, interface, logic, and optoelectronics products. Please contact us on the web at www.fairchildsemi.com.

Special Note on Forward-Looking Statements and Risk Factors:
This news release contains forward-looking statements, including those regarding our ability to successfully satisfy the conditions to complete the acquisition including the share swap and merger. These statements are based on management's assumptions and expectations, which involve risk and uncertainty. Many factors could cause actual results to differ materially from those expressed in forward-looking statements. These factors include, but are not limited to, our ability to consummate and satisfy the conditions to closing the share swap and merger; our ability to successfully address the challenges associated with integrating this acquisition; and our ability to retain and develop System General's markets, facilities and personnel. System General is currently appealing the outcome of proceedings before the U.S. International Trade Commission (ITC) involving allegations of patent infringement, and is a defendant in a patent infringement lawsuit in the U.S. District Court for the Northern District of California. Both the ITC proceeding and the lawsuit were initiated by Power Integrations, Inc. As in all litigation, the results of these matters are difficult to predict and no assurance can be given as to the outcome of these proceedings. An adverse outcome in these matters after completion of the acquisition could negatively impact our financial results. We are also involved in patent infringement litigation against Power Integrations in U.S. district courts in Delaware and Texas, as a defendant and as a plaintiff, respectively. These lawsuits and risk factors, and other risk factors as they relate to Fairchild are discussed in the company's quarterly and annual reports filed with the SEC and are available at the Investor Relations section of Fairchild web site at www.fairchildsemi.com or the SEC's web site at www.sec.gov.

Exhibit N

ORRICK

ORRICK, HERRINGTON & SUTCLIFFE LLP
1000 MARSH ROAD
MENLO PARK, CALIFORNIA 94025
tel 650-614-7400
fax 650-614-7401
WWW.ORRICK.COM

December 9, 2005

Bas de Blank
(650) 614-7343
basdeblank@orrick.com

VIA FACSIMILE

Michael Headley
Fish & Richardson P.C.
500 Arguello Street
Suite 500
Redwood City, CA 94036

Re: Power Integrations v. Fairchild Semiconductor et al. (CA 04-1371 JJF)

Dear Michael:

I write to supplement Fairchild's proposed claim construction. In light of Mr. Balakrishnan's recent testimony and upon further discussions with our experts, we do not believe that the soft start circuit element of the '366 and '851 patents should be construed in means-plus-function terms. Thus, I have supplemented the proposed constructions the parties have previously exchanged.

Further, in an effort to simplify matters, Fairchild does not dispute Power Integrations proposed construction of "Maximum duty cycle signal comprising an on-state and an off-state". This also obviates the need to construe "on-state" and "off-state" separately. Finally, Fairchild agrees with Power Integrations that the term "said maximum duty cycle" should be given its plain, English-language interpretation and does not need to be construed by the Court.

I have attached a chart of the remaining terms that are in dispute, along with each parties' proposed constructions. Please do not hesitate to call should you have any questions.

Sincerely,

Bas de Blank

cc: William J. Marsden, Jr.
Howard G. Pollack

ORRICK

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1000 MARSH ROAD
MENLO PARK, CALIFORNIA 94025
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WWW.ORRICK.COM

FAX TRANSMISSION

DATE December 9, 2005

NO. OF PAGES (INCLUDING COVER SHEET) 10

FROM name	tel
Bas de Blank	650-614-7343

TO name	company/firm	tel	Fax
Michael Headley	FISH & RICHARDSON P.C.		650.839.5071
CC			
William J. Marsden, Jr.	FISH & RICHARDSON P.C.		302.652-0607
Howard G. Pollack	FISH & RICHARDSON P.C.		650.839.5071

RE *Power Integrations v. Fairchild Semiconductor et al*

MESSAGE

Please see attached.

C-M-A 10414-25/7584

IF YOU DO NOT RECEIVE ALL PAGES, PLEASE CALL MIMI SAGMIT AT (650) 614-7451 AS SOON AS POSSIBLE.

Term	Fairchild's Construction	Power Integrations' Construction	'075 Claim
MOS transistor	A metal-oxide-semiconductor transistor having the elements set forth in the claim, which excludes a DMOS transistor.	A MOS transistor is a metal-oxide-semiconductor device that can control the flow of current between a source terminal and a drain terminal. In common usage in the industry, "high voltage" generally refers to a device that can operate at 50V and above. Power Integrations disagrees with Fairchild that this term, or this claim, excludes all application to devices that may be referred to as "DMOS" transistors.	1, 5
substrate	The physical material on which a transistor is fabricated.	A substrate as expressly defined in the '075 patent is the physical material on which a microcircuit is fabricated and may include subsequently formed or doped regions which are expressly provided for in the patent and referred to as a "secondary substrate" such as a well or epitaxial layer.	1
a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate	Two laterally spaced pockets of semiconductor material of the opposite conductivity type from the substrate present within the physical material on which a microcircuit is fabricated. Power Integrations disclaimed reading this element on a DMOS transistors.	"[P]air of laterally spaced pockets of semiconductor material of a second conductivity type" should be given its plain, English language meaning. "Within the substrate" refers to anywhere within the boundaries of the substrate. Such a pocket can be within a well region and still be "within the substrate" as recited in the claim. Power Integrations disagrees with Fairchild that this phrase, or this claim, excludes all application to devices that may be referred to as "DMOS" transistors.	1
adjoining	To be very near, next to, or touching.	To be very near, next to, or touching.	1
a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain	A layer of material of the same conductivity as the substrate above a portion of the extended drain region and between the drain contact pocket and each of the surface adjoining positions of the extended drain region. Power	Power Integrations does not believe this term requires construction. It should be subject to plain, English-language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction:	1

Term	Fairchild's Construction	Power Integrations' Construction	Claim
region between the drain contact pocket and the surface-adjoining positions	Integrations disclaimed reading this element on a DMOS transistor.	A layer of material of the same conductivity type as the substrate located on top of a portion of the extended drain region between the drain contact pocket and surface adjoining positions of the extended drain region. Power Integrations disagrees with Fairchild that this phrase, or this claim, excludes all application to devices that may be referred to as "DMOS" transistors.	
said top layer of material	This term lacks antecedent basis and cannot be construed.	Power Integrations does not believe this term requires construction. It should be subject to plain, English-language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction: The top layer of material in this limitation refers to the surface adjoining layer.	1
substrate region thereunder which forms a channel	A channel is formed laterally in the substrate between the source contact pocket and the nearest surface-adjoining position of the extended drain region. Power Integrations disclaimed reading this element on a DMOS transistor.	This phrase should be afforded its plain meaning and simply refers to the physical location of the "channel" being formed underneath the gate region. Nothing in the patent precludes the channel from being formed in "well" material or otherwise doped material beneath the insulated gate. Power Integrations disagrees with Fairchild that this phrase, or this claim, excludes all application to devices that may be referred to as "DMOS" transistors.	1
being subject to application of a reverse-bias voltage	Experiencing a bias voltage applied to a semiconductor junction with polarity that permits little or no current to flow.	Reverse-bias in this context is a voltage applied across a rectifying junction with a polarity that provides a high-resistance path. It means that the surface adjoining layer of material recited in the claims is connected in some way to the substrate or "ground" potential.	1

Term	Fairchild's proposed construction	Power Integrations' proposed construction	'066 Claim	'851 Claim	'876 Claim
frequency jittering	Frequency jitter is an intentional modulation or variation in the frequency of a signal.	Frequency jitter in the context of the patent is a controlled and predetermined change or variation in the frequency of a signal.			1
coupled	Two circuits are coupled when they are configured such that signals pass from one to the other	Power Integrations does not believe this term requires construction. It should be subject to plain, English-language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction: Two circuits are coupled when they are connected such that voltage, current, or control signals pass from one to the other.	8, 18	9, 11, 17	1
primary voltage	The voltage generated by the primary voltage source.	A primary voltage is a base or initial voltage. Nothing in the patent limits this term to a voltage generated solely by a "primary voltage source."			17, 19
cycling	A periodic change of the controlled variable.	Power Integrations does not believe this term requires construction. It should be subject to plain, English-language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction: Cycling is repeating a sequence or a pattern			17
secondary voltage sources	Additional voltage sources distinct from the primary voltage source.	A voltage source is a source, i.e. a place of procurement or a supply, of voltage and may			17, 19

		include, for example, a resistor having a substantially constant current flowing through it. A secondary voltage source is a source of a secondary voltage. Nothing in the claims or specification requires the secondary voltage source be independent from the source of the primary voltage.			
secondary voltage	A voltage generated by the secondary voltage sources.	Plain meaning: secondary voltage is a subsequent or additional voltage.			17
combining	Adding together from two or more different sources.	Power Integrations does not believe this term requires construction. It should be subject to plain, English-language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction: Combining means adding together. There is nothing that requires the "different sources" added limitation of Fairchild's proposed construction.			17
supplemental voltage	A voltage other than the primary or secondary voltages.	Power Integrations does not believe this term requires construction. It should be subject to plain, English-language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction: A voltage in addition to the primary voltage. Nothing in the intrinsic evidence suggests that a			19

		"supplemental voltage" must be different from the "secondary" voltage.			
Soft start circuit	A circuit that minimizes inrush currents at start up.	Soft start circuit should be construed according to 35 U.S.C. § 112 ¶ 6 to include the circuit structures disclosed in the specification for performing the recited functions, and equivalents thereof. The corresponding structures for the "soft start circuit" are disclosed in the specification of the '851 patent at: Col. 5, line 66 – Col. 6, line 9; Col. 6, lines 25-Col. 7, line 8; Col. 11, line 64-Col. 12, line2. The specification expressly excludes from the definition of "soft start circuit" prior art circuits using an external "soft start capacitor." *See* Col. 2, line 58-Col. 3, line 8.	1, 2, 9, 16	4, 13	
soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said on-state of said maximum duty cycle	A circuit that minimizes inrush currents at start up by providing a signal instructing the drive circuit to disable the drive signal during at least a portion of the on-state of the maximum duty cycle signal. Fairchild does not believe this to be a means-plus-function term. Should the Court determine this to be a means-plus-function element, however, it should be construed to mean a structure that provides the functionality of providing a signal instructing said drive circuit to disable said drive signal during at least a portion of said on-state of said	The functionality should be construed in accordance with the plain meaning of its terms. The corresponding structure is the same as set forth above.	1, 2		

Term	Fairchild's Construction	Power Integrations' Construction	'366 Claim	'851 Claim	'576 Claim
	maximum duty cycle. This means-plus-function element is limited to the structure disclosed in the '366 and '851 patents, and equivalents thereof. The only such structures disclosed are (i) the circuit shown in Figure 1, including capacitor 110, (ii) the soft start block and low frequency oscillator shown in Figures 3, 6, and 9, and (iii) the corresponding portions of the specification describing these structures.				
a soft start circuit that provides a signal instructing said drive circuit to discontinue said drive signal according to a magnitude of said frequency variation signal	A circuit that minimizes inrush currents at start up by providing a signal instructing the drive circuit to disable the drive signal according to a magnitude of the frequency variation signal. Fairchild does not believe this to be a means-plus-function term. Should the Court determine this to be a means-plus-function element, however, it should be construed to mean a structure that provides the functionality of providing a signal instructing said drive circuit to discontinue said drive signal according to a magnitude of said frequency variation signal. This means-plus-function element is limited to the structure disclosed in the '366 and '851 patents, and equivalents thereof. The only such structures disclosed are the soft start block and low frequency oscillator shown in Figures 3, 6, and 9, and (iii) the corresponding portions of the specification describing these structures.	The functionality should be construed in accordance with the plain meaning of its terms. The corresponding structure is the same as set forth above re soft start circuit.		13	
a soft start	A circuit that minimizes	The functionality should	9, 16		

[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said maximum time period	inrush currents at start up by providing a signal instructing the drive circuit to disable the drive signal during at least a portion of the maximum time period. Fairchild does not believe this to be a means-plus-function term. Should the Court determine this to be a means-plus-function element, however, it should be construed to mean a structure that provides the functionality of providing a signal instructing said drive circuit to disable said drive signal during at least a portion of said maximum time period. This means-plus- function element is limited to the structure disclosed in the '366 and '851 patents, and equivalents thereof. The only such structures disclosed are (i) the circuit shown in Figure 1, including capacitor 110, (ii) the soft start block and low frequency oscillator shown in Figures 3, 6, and 9, and (iii) the corresponding portions of the specification describing these structures.	be construed in accordance with the plain meaning of its terms. The corresponding structure is the same as set forth above re soft start circuit.			
a soft start circuit that provides a signal instructing said drive circuit to discontinue said drive signal when said magnitude of said oscillation signal is greater than a magnitude of said frequency	A circuit that minimizes inrush currents at start up by providing a signal instructing the drive circuit to discontinue the drive signal when the magnitude of the oscillation signal is greater than a magnitude of the frequency variation signal. Fairchild does not believe this to be a means-plus-function term. Should the Court determine this to be a means-plus-function element, however, it should be construed to mean a structure	The functionality should be construed in accordance with the plain meaning of its terms. The corresponding structure is the same as set forth above re soft start circuit.		4	

Term	Corrected Construction	Court's Construction	'366 Claim	'851 Claim	'276 Claim
variation signal	that provides the functionality of providing a signal instructing said drive circuit to discontinue said drive signal when said magnitude of said oscillation signal is greater than a magnitude of said frequency variation signal. This means-plus-function element is limited to the structure disclosed in the '366 and '851 patents, and equivalents thereof. The only such structures disclosed are (ii) the soft start block and low frequency oscillator shown in Figures 3, 6, and 9, and (iii) the corresponding portions of the specification describing these structures.				
monolithic device	A device constructed from a single crystal or other single piece of material.	A device constructed from a single crystal or other single piece of material.	2, 16	2, 16	
frequency variation circuit that provides a frequency variation signal	A structure that provides the functionality of providing a signal that is used to modulate or change the frequency at which the switch is operated. This means-plus-function element is limited to the structure disclosed in the '366 and '851 patents, and equivalents thereof. The only such structures disclosed are (i) the circuit shown in Figure 1 including resistor 140 and current 135, (ii) the frequency variation block and low frequency oscillator shown in Figures 3, 6, and 9, and (iii) the corresponding portions of the specification describing these structures.	A frequency variation circuit is a structure that provides the "frequency variation signal". A frequency variation signal is an internal signal that cyclically varies in magnitude during a fixed period of time and is used to modulate the frequency of the oscillation signal within a predetermined frequency range.	5, 14	1, 2, 11, 16	